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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,498	03/23/2004	Mieu Van Vu	SC12998TH	2772

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EXAMINER	
LE, NHAN T	

ART UNIT	PAPER NUMBER
2685	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,498	VU ET AL.	
	Examiner	Art Unit	
	Nhan T Le	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 15-21* is/are rejected.

7)☒ Claim(s) *11-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/23/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-8, 15-17, 20, 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Leclercq (US 2004/0248624).

As to claims 1, 20, Leclercq teaches a method for entering a low power mode, comprising: providing a first power control mode indicator to a first power control stage (see fig. 3, block 305, paragraphs 0033-0037), the first power control mode indicator selecting a first low power mode (see fig. 3, ckvtcxo_in, paragraphs 0033-0037); receiving a trigger input signal at the first power control stage triggering at least a first module to enter the first low power mode (see fig. 3, input from block 340, paragraphs 0033-0037); providing a first request signal requesting the first module to enter the first low power mode based on the trigger input signal (see fig. 3, clr_deep_sleep, paragraphs 0033-0037); providing a first response signal indicating that the first module is ready to enter the first low power mode (see fig. 3, input line between blocks 310 and 350, paragraphs 0033-0037); and providing a first control signal in response to the first response signal, the first control signal enabling low power features corresponding to

the first low power mode (see fig. 3, control line between blocks 305 and 350, paragraphs 0033-0037).

As to claims 2, 3, 21, Leclercq teaches comprising deasserting the first request signal based on the first control signal and wherein the first request signal is an interrupt holdoff signal (see fig. 3, sys_clk13M, paragraph 0035).

As to claim 4, Leclercq teaches wherein the low power features include at least one of clock gating, reducing voltage, power gating (see fig. 3, sys_clk13M, paragraph 0035).

As to claims 5-6, Leclercq teaches wherein the first module is a power master; wherein the power master is at least one of a microcontroller (see paragraph 0036).

As to claims 7, 8, Leclercq teaches further comprising enabling at least a portion of the low power features that are internal to the power master based on the first request signal and wherein the step of deasserting the first request signal is performed using a first feedback output signal and a first feedback input signal, wherein first feedback output signal is provided by the first power control stage (see fig. 3, sys_clk13M, paragraph 0035).

As to claim 15, Leclercq teaches an apparatus for entering a low power mode, comprising: a first module (see fig. 3, block 310, paragraphs 0033-0037); a first power control stage coupled to the first module (see fig. 3, block 305, paragraphs 0033-0037); a first power control mode indicator provided to the first power control stage mode (see fig. 3, ckvtcxo_in, paragraphs 0033-0037), the first power control mode indicator selecting a first low power mode; a trigger input signal (see fig. 3, input from block 340,

paragraphs 0033-0037) received at the first power control stage triggering at least the first module to enter the first low power mode; a first request signal (see fig. 3, clr_deep_sleep, paragraphs 0033-0037) requesting the first module to enter the first low power mode, the first request signal based on the trigger input signal; a first response signal (see fig. 3, input line between blocks 310 and 350, paragraphs 0033-0037) indicating that the first module is ready to enter the first low power mode; and a first control signal provided in response to the first response signal, the first control signal enabling low power features corresponding to the first low power mode, wherein the first request signal is deasserted based on the first trigger input signal (see fig. 3, control line between blocks 305 and 350, paragraphs 0033-0037).

As to claim 16, Leclercq teaches wherein the first module is a power master being the low power features include at least one of clock gating, reducing voltage, power gating (see fig. 3, sys_clk13M, paragraph 0035), and the low power mode is at least one of a WAIT mode and a Deep Sleep Mode (DSM) (see paragraphs 0033-0037).

As to claim 17, Leclercq teaches wherein the deassertion is performed using a first feedback output signal and a first feedback input signal, wherein first feedback output signal is provided by the first power control stage (see fig. 3, sys_clk13M, paragraph 0035).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 9, 10, 18, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leclercq (US 2004/0248624) in view of Kenny et al (US 5,954,819).

As to claims 9, 10, Leclercq fails to teach providing a first trigger output signal to a second power control stage, providing the first feedback input signal using a second feedback output signal, and providing the second feedback output signal using the first trigger output signal; wherein the second feedback output signal is provided using a second power control mode indicator corresponding to the second power control stage. Kenny teaches comprising providing a first trigger output signal to a second power control stage, providing the first feedback input signal using a second feedback output signal, and providing the second feedback output signal using the first trigger output signal wherein the second feedback output signal is provided using a second power control mode indicator corresponding to the second power control stage (see fig. 3b, clk1, clk2, clk3, col. 6, lines 10-28). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Kenny into the system of Leclercq in order to limit the power consumption by controlling the clock stopping signals.

As to claims 18, 19, the claims are rejected as to claims 9, 10 above.

Allowable Subject Matter

Claims 11-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As to claim 11, the applied reference fails to teach providing the second power control mode indicator to the second power control stage, the second power control mode indicator selecting a second low-power mode, receiving the first trigger output signal at the second power control stage triggering at least a second module to enter the second low power mode, providing a second request signal requesting the second module to enter the second low power mode based on the first trigger output signal, providing a second response signal indicating that the second module is ready to enter the second low power mode, providing a second control signal in response to the second response signal, the second control signal enabling the low power features corresponding to the second low power mode, and deasserting the second request signal based on the second control signal.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Marx et al (US 6,725,067) teaches method and system for restarting a reference clock of a mobile station after a sleep period with zero mean time error.

Moyer et al (US 2003/0172310) teaches low power system and method for a data processing system.

Shohara et al (US 6,804,503) teaches communication device with a self-calibrating sleep timer.

Cannon et al (US 2003/0032463) teaches extended power saving for electronic device.

Jain et al (US 2003/0172313) teaches sleep state transitioning.

Kojima et al (US 2004/0203389) teaches wireless communication system and microcomputer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T Le whose telephone number is 571-272-7892. The examiner can normally be reached on 08:00-05:00 (Mon-Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on 571-272-7899. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

N.Le

Nhan Le

Nguyen Vo
10_30_2005

NGUYEN T. VO
PRIMARY EXAMINER